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EXAMINER	
CHIO, TAT CHI	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 10/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/064,352	CHEN, KUAN-CHOU	
	Examiner	Art Unit	
	Tat Chi Chio	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-17 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-17 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 2, 3, 4, 6, 7, and 8 are rejected under 35 U.S.C. 102(e) as being anticipated by Cho (US 6,859,614 B1).

Regarding claim 1, an electronic circuit comprising: a servo control and ECC decoder circuit for controlling a removable media device to obtain encoded data from a removable media, and for performing a decoding process to obtain decoded data from the encoded data and storing the decoded data in an external memory; a graphics decoding circuit for decoding graphics data held in the external memory to generate video data and audio data; and a memory controller to provide read and write access to the external memory for both the servo control and ECC decoder circuit and the graphics decoding circuit; wherein the graphics decoding circuit performs a graphics decoding process on the decoded data to generate the video data and audio data.

Cho discloses a disk motor for rotating a DVD at a constant linear velocity to reproduce an image recorded on the disk (see col. 4, line 30-35), an ECC (error correction circuit) for correcting errors in the row and column directions in the data read

from the DVD (see col. 4, line 63-65), an audio/video decoder for dividing the data output from the system decoder into audio and video data (see col. 1, line 65-66), and a memory controller for connecting to the memory and devices via a data/address bus (see col. 3, line 15-20).

Claim 2 further limits the graphics decoding circuit of claim 1 to a memory controller to store the video data in the external memory.

Cho discloses that the memory controller addresses the memory under the control of the microcomputer and stores corresponding demodulated data into the memory (see col. 5, line 6-8).

Claim 3 further limits the electronic circuit in of claim 1 to comprise video output circuitry for generating a video signal for an external display device according to the video data.

Cho discloses that the demodulated audio and video data output from the audio/video decoder are transferred to a speaker and a monitor, respectively, via a digital-to-analog converter and an NTSC encoder (see col. 1, line 66-67 and col. 2, line 1-3).

Claim 4 further limits the electronic circuit of claim 1 to comprise a communications pathway electrically linking the Servo control and ECC decoder circuit with the graphics decoding circuit to permit the servo control and ECC decoder circuit and the graphics decoding circuit to exchange information.

Cho discloses that the ECC forms a communication path with the data bus to access the memory (see col.5, line 14-17) and the A/V decoder interface and DVD-

ROM interface forms a communication path with the data bus to access the memory (see col. 5, line 41-45). Therefore, the ECC and A/V decoder are able to communicate with each other by accessing the memory.

Claim 6 further limits the servo control and ECC decoder circuit of claim 4 to comprise a signal to indicate to the graphics decoding circuit that newly decoded data is available in the external memory.

Cho discloses that a microcomputer register receives data output from the microcomputer to store various control signals for controlling each part of the system decoder, and stores state information generated from each part of the system decoder to provide the microcomputer with the state information (see col. 6, line 15-20).

Claim 7 further limits the servo control and ECC decoder circuit of claim 1 to decode data received from a digital video disk (DVD) removable media, or a compact disk (CD) removable media.

Cho discloses that an ECC decoder corrects errors in the row and column directions, with respect to a predetermined error correction block, in the data read from the DVD, which is essentially the function of an ECC decoder (see col. 4, line 63-65).

Claim 8 further limits the servo control and ECC decoder circuit of claim 7 to control a DVD-type drive, or a CD-type drive.

Cho discloses that a disk motor rotates a DVD at a constant linear velocity, with respect to a head, to reproduce an image recorded on the disk (see col. 4, line 31-35).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cho (US 6,859,614 B1) in view of Chau (US 5,870,087) and Haratsch et al (US 6,154,222).

Claim 9 further limits the graphics decoding circuit of claim 1 to a Moving Picture Experts Group (MPEG) type graphics decoding process to generate the video data.

Cho teaches all the limitations as stated in claim 1, but Cho fails to explicitly disclose that the graphics decoding circuit performs a Moving Picture Experts Group (MPEG) type graphics decoding process to generate the video data.

Chau teaches a video decoding system that includes a single unified memory, which stores code and data for the transport logic, system controller and MPEG decoder functions (see col. 5, line 3-6).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have used a MPEG decoder to generate the video data since Haratsch et al. teach that "The major advantage of MPEG over other video and audio standard is said to be much smaller file size for the same quality due to the efficient compression technique employed" (see col. 1, line 30-35 of Haratsch et al.).

5. Claims 10 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cho (US 6,859,614 B1) in view of Romano et al (US 5,586,306) and Casalnuovo et al (US 6,232,139 B1).

Claim 10 further limits the electronic circuit of claim 1 to comprise a monolithic substrate, the removable media device driver and decoder circuit, the graphics decoding circuit and the memory controller all fabricated on the monolithic substrate.

Cho teaches all the limitations as stated in claim 1, but Cho fails to explicitly disclose that the removable media device driver and decoder circuit, the graphics decoding circuit and the memory controller all fabricated on the monolithic substrate.

Romano et al teach a single monolithic integrated circuit embodying all or substantially all of the motion control and processing functionality of a disk drive (see col. 3, line 1-4).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have fabricated the removable media device driver and decoder circuit, the graphics decoding circuit and the memory controller on the monolithic substrate since Casalnuovo et al teach that "The advantages of monolithic integration are widely recognized and include: smaller size, greater functionality, lower power requirements, improved reliability, tighter manufacturing tolerances, and simplified packaging" (see col. 8, line 10-14).

Regarding claim 12, an electronic circuit fabricated on a monolithic substrate comprise: a servo control and ECC decoder circuit for controlling a removable media device to obtain encoded data from a removable media, and for performing a decoding

process to obtain decoded data from the encoded data and storing the decoded data in an external memory; a graphics decoding circuit for decoding graphics data held in the external memory to generate video data and audio data; a memory controller to provide read and write access to the external memory for both the servo control and ECC decoder circuit and the graphics decoding circuit; and a communications pathway enabling the servo control and ECC decoder circuit, the graphics decoding circuit and the memory controller to exchange information with each other.

Cho explicitly discloses a disk motor for rotating a DVD at a constant linear velocity to reproduce an image recorded on the disk (see col. 4, line 30-35), an ECC (error correction circuit) for correcting errors in the row and column directions in the data read from the DVD (see col. 4, line 63-65), an audio/video decoder for dividing the data output from the system decoder into audio and video data (see col. 1, line 65-66), and a memory controller for connecting to the memory and devices via a data/address bus (see col. 3, line 15-20). Cho also discloses that the ECC forms a communication path with the data bus to access the memory (see col.5, line 14-17) and the A/V decoder interface and DVD-ROM interface forms a communication path with the data bus to access the memory (see col. 5, line 41-45). Therefore, the ECC, memory controller, and A/V decoder are able to communicate with each other by accessing the memory. However, Cho fails to explicitly disclose that the electronic circuit is fabricated on a monolithic substrate.

Romano et al teach a single monolithic integrated circuit embodying all or substantially all of the motion control and processing functionality of a disk drive (see col. 3, line 1-4).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have fabricated the removable media device driver and decoder circuit, the graphics decoding circuit and the memory controller on the monolithic substrate since Casalnuovo et al teach that "The advantages of monolithic integration are widely recognized and include: smaller size, greater functionality, lower power requirements, improved reliability, tighter manufacturing tolerances, and simplified packaging" (see col. 8, line 10-14).

6. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cho (US 6,859,614 B1) in view of Washida et al (US 6,239,981 B1) and Yano et al (US 5,463,248).

Claim 11 further limits the electronic circuit of claim 1 to comprise a packaging substrate, the removable media device driver and decoder circuit, the graphics decoding circuit and the memory controller all disposed within the packaging substrate.

Cho teaches all the limitations as stated in claim 1, but Cho fails to explicitly disclose that the removable media device driver and decoder circuit, the graphics decoding circuit and the memory controller all disposed within the packaging substrate.

Washida et al teach that a packaging substrate on which electronic components having a plurality of connecting terminals at their side edge portions and other kind of

electronic component can be mounted in high density on the substrate (see col. 2, line 30-36).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have disposed the removable media device driver and decoder circuit, the graphics decoding circuit and the memory controller within the packaging substrate since Yano et al teach that a package substrate made of aluminum nitride exhibits an outstanding heat radiating property (see col. 4, line 12-18 of Yano et al.).

7. Claims 15, 16, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cho (US 6,859,614 B1) in view of Romano et al (US 5,586,306), Casalnuovo et al (US 6,232,139 B1), Iwamura (5,838,876), and Kim et al (US 7,042,948 B2).

Claim 15 further limits the graphics decoder circuit of claim 12 to comprises: a video head pointer indicating a first address where a newest video data is stored in the external memory; an audio head pointer indicating a second address where a newest audio data is stored in the external memory; a video tail pointer indicating a third address where an oldest video data is stored in the external memory; an audio tail pointer indicating a fourth address where an oldest audio data is stored in the external memory, wherein the video head pointer and the video tail pointer constitute a video circular buffer in the external memory, and the audio head pointer and the audio tail pointer constitute an audio circular buffer in the external memory.

Claim 16 further limits the graphics decoder circuit of claim 15 to stop the graphics decoding process when either the video head pointer is about to write over the

video tail pointer or the audio head pointer is about to write over the audio tail pointer, so as to prevent loss of the video data or the audio data respectively.

Claim 17 further limits the graphics decoder circuit of claim 15 to resume the video tail pointer when the video tail pointer advances close enough to the video head pointer, or resumes the audio tail pointer when the audio tail pointer advances close enough to the audio head pointer.

Cho, Romano et al, and Casalnuovo et al teach all the limitations as stated in claim 12, but they fail to explicitly disclose that a circular buffer is used in the external memory.

Iwamura explicitly discloses a ring buffer is used in the memory. A write pointer indicates the memory address within ring buffer at which incoming data is to be written, and a read pointer indicates the address of ring buffer from which data is to be read out for storage (see col. 5, line 38-50). Furthermore, writing to the buffer stops just before ring buffer would overflow (see col. 5, line 55-56), and when the amount of data remaining in buffer falls below a preset threshold, writing resumes (see col. 6, line 7-9).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have used a ring buffer in the external memory since Kim et al teach that "The ring buffer provides fast and efficient access to video bitstream data that may be accessed multiple times in multiple directions by modules that extract data from the video bitstream in an error resilient manner (see col. 2, line 35-40 of Kim et al).

8. Claim 5, 13, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cho (US 6,859,614 B1) in view of Yuen et al (US 2003/0190138 A1).

Claim 5 further limits the servo control and ECC decoder circuit of claim 4 to comprise a register accessible by the graphics decoding circuit that indicates the location of decoded data in the external memory.

Cho teaches all the limitations in claim 4, but Cho fails to explicitly disclose a register accessible by the graphics decoding circuit that indicates the location of decoded data in the external memory.

Yuen et al teach that a directory controller that indicates the location of the video program (see Fig. 5).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have used a directory controller to indicate the location of the video program since Yuen et al teach that "the availability of a program directory will eliminate much of the frustration that has been felt for so long by so many users of tape devices" (see [0022] of Yuen et al.).

Claim 13 further limits the servo control and ECC decoder circuit of claim 1 to comprise: a first register indicating a first storage location in the external memory for the encoded data from the removable media; a second register indicating a second storage location in the external memory for the decoded data which is decoded from the encoded data; and a third register indicating a size of the decoded data.

Cho teaches all the limitations in claim 4, but Cho fails to explicitly disclose a register accessible by the graphics decoding circuit that indicates the location and the size of decoded data in the external memory.

Yuen et al teach that a directory controller that indicates the location and the length of the video program (see Fig. 5).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have used a directory controller to indicate the location of the video program since Yuen et al teach that "the availability of a program directory will eliminate much of the frustration that has been felt for so long by so many users of tape devices" (see [0022] of Yuen et al.).

Claim 14 further limits the electronic circuit claim 13 that the second storage location overlaps the first storage location.

Yuen et al teach that the controller adjusts the length due to overlap of programs. Therefore, the programs overlap each other (see [0875] of Yuen et al.).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tat Chi Chio whose telephone number is (571) 272-9563. The examiner can normally be reached on Monday - Friday 7:30 AM-5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey Stucker can be reached on (571) 272-0911. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TC

JEFFREY STUCKER
SUPERVISORY PATENT EXAMINER